AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8. (Canceled)

9. (Currently Amended) A method for improving the reliability of a computer system including ~~a bus, an interface circuit, and~~ a bus and at least one plug-in unit ~~which is connected to the bus via the interface circuit~~ coupled thereto, comprising:

providing to each of at least one plug-in unit a separate interface circuit such that each said plug-in unit is connected to said bus via said interface circuit corresponding thereto;

addressing ~~the~~ a respective plug-in unit, via the bus, by addressing operations directed at said respective ~~the~~ plug-in unit and which are monitored by ~~the~~ said interface circuit corresponding thereto;

~~measuring a duration of addressing of the plug-in unit; and when the duration exceeds a predetermined period of time, then the addressing is terminated by sending into the bus a signal indicating termination of addressing~~

performing a time duration operation of addressing of said plug-in unit; and

checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before expiration of a predetermined period of time, the time duration operation of addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing, and (ii) when the duration operation of addressing exceeds the

predetermined time period, the addressing to that plug-in unit is terminated by said interface circuit corresponding thereto by sending into the bus a signal indicating termination of addressing.

10. (Currently Amended) A method as defined in claim 9, wherein:

the time duration of addressing is monitored using a watchdog timer with a predetermined timing set therein.

11. (Previously Presented) A method as defined in claim 9, wherein:

when addressing is terminated an error signal is set by the interface circuit into an active state in the bus.

12. (Previously Presented) A method as defined in claim 9, wherein:

when addressing is terminated an error signal indicating an error condition in the plug-in unit is set by the interface circuit into an active state in the status register of the plug-in unit.

13. (Currently Amended) An interface circuit for ~~improving the reliability~~ providing local monitoring capability to a plug-in unit of a computer system including a ~~bus, and a~~ bus and at least one plug-in unit ~~which is connected to the bus via the interface circuit, the interface circuit~~ coupled to said bus; wherein a separate interface circuit is provided to connect each said plug-in unit to said bus and comprising:

a watchdog timer;

~~means for starting the watchdog timer upon the start of addressing; and~~

~~means for sending into the bus a signal indicating termination of addressing~~

first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto; and

second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

14. (Currently Amended) An interface circuit as defined in claim 13, further comprising:

means for setting an error signal into an active state in the bus.

15. (Currently Amended) An interface circuit as defined in claim 13, further comprising:

means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit.

16. (Currently Amended) An interface circuit as defined in claim 14, further comprising:

means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit.

17. (Currently Amended) An interface circuit as defined in claim 13, ~~where~~wherein:

the bus is a Compact PCI bus.

18. (New) An interface circuit as defined in claim 16, wherein:

the bus is a Compact PCI bus.

19. (New) An interface circuit as defined in claim 13, wherein:

each said interface circuit is provided as a part of said plug-in unit corresponding thereto.

20. (New) A method according to claim 10, wherein:

said watchdog timer is provided at each said interface circuit or at each said plug-in unit.

21. (New) A computer system including a bus and at least one plug-in unit coupled thereto, wherein the improvement comprises:

providing at least one interface circuit and at least one plug-in unit each of which is connected to said bus via a separate said interface circuit corresponding thereto, wherein each said interface circuit comprises:

a watchdog timer;

first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto; and

second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

22. (New) A computer system according to claim 21, wherein each said interface further comprises:

means for setting an error signal into an active state in the bus.

23. (New) A computer system according to claim 22, wherein each said interface circuit comprises:

means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit.

24. (New) A computer system according to claim 23, wherein:

the bus is a Compact PCI bus.

25. (New) A computer system according to claim 21, wherein each said interface circuit comprises:

means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit.

26. (New) A computer system according to claim 21, wherein:

the bus is a Compact PCI bus.

27. (New) A computer system according to claim 21, wherein:

each said interface circuit is provided as a part of said plug-in unit corresponding thereto.

28. (New) A computer system according to claim 27, wherein:

the bus is a Compact PCI bus.